FP 13.1: A 70Mb/s Variable-Rate 1024-QAM Cable Receiver IC with Integrated 10b ADC and FEC Decoder

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A variable-rate IF-sampled QAM receiver integrated circuit operates at symbol rates from 1 to 7MBaud in 4, 16, 32, 64, 128, 256, and 1024-QAM. The QAM receiver is a monolithic mixed-signal device implemented in a 0.5µm triple-level metal single-poly CMOS process. The device incorporates a 10b A/D converter, analog PLLs, interpolating demodulator, square-root raised cosine receive filters, timing/carrier recovery loops, 20-tap complex equalizer, and a Reed-Solomon forward error correction (FEC) decoder that is compliant with European digital video broadcasting (DVB) and Digital Audio-Visual Council (DAVIC) standards [1]. Applications of this QAM receiver include digital cable-TV set-top terminals, cable modems, and digital microwave radios.

A top level functional block diagram of the QAM receiver including an RF front-end is illustrated in Figure1. The integrated 10b A/D converter of the QAM receiver accepts a 2 V_{pp} differential input up to 32MHz sampling rate. The digitized IF_2 centered data stream from the A/D converter is demodulated to baseband in-phase (I) and quadrature (Q) channels by down-mixing with $\cos(\pi n/2)$ and $\sin(\pi n/2)$ [2].

The A/D converter is clocked by a crystal referenced integrated PLL at a fixed rate incommensurate with the symbol rate of the receiver. The reconstruction and symbol timing recovery uses a polynomial interpolator [3]. Given two successive input samples b(n) and b(n+1), the interpolator produces any sample b(n+µ) where µ is a fractional valued interpolation interval generated by the symbol timing recovery 2nd-order digital PLL. The resulting timing-recovered data stream at the output of the interpolator is filtered by a complex receive filter, implemented using a canonic signed digit (CSD) architecture [2].

A wideband decision-directed carrier-recovery loop removes residual carrier frequency offsets and tracks phase noise produced by the RF tuner. The phase discriminant is filtered by an integral-plus-proportional loop filter where the output drives a quadrature direct digital frequency synthesizer (QDDFS) [4]. The measured tracking bandwidth of the phase derotator loop exceeds 100kHz at 5MBaud operation.

The complex equalizer consists of two transpose-form adaptive FIR filters - an 8-tap feedforward (FFE) filter and a 12-tap decision feedback (DFE) filter. Each filter employs a parallel-tap architecture that allows simple control distribution and data propagation, as well as convenient scalability for applications requiring different equalizer spans (Figure 2). The 12-tap DFE enables the receiver to correct multipath with delays in excess of 1.7µs for 7MBaud operation. The equalizer can be configured to provide radio frequency interference (RFI) cancellation. The sign-LMS coefficient update is distributed among the filter taps, localizing the coefficient storage and further minimizing the global signal overhead. The fundamental computational core of the equalizer is the adaptive tap, consisting of an LMS update block, a multiplier, and an accumulator (Figure 3). Each tap performs one complex multiply-accumulate operation plus one complex coefficient update per symbol period using a single multiplier and two adders time-shared 4 times.

The FEC decoder consists of 4 blocks: frame synchronization, convolutional deinterleaving, Reed-Solomon (RS) error correction, and derandomization. The frame synchronization block recovers MPEG framed data streams as defined in the DVB and DAVIC specification. The programmable convolutional deinterleaver is compatible with the Ramsey type III approach. The interleaving depth, I, is programmable from I=1-12, 204 where I divides 204. An on-chip RAM is provided for I=1-12 and control is supplied for an off-chip RAM for I>12. The RS decoder processes the t = 8(n,k) = (204,188) shortened RS code, defined by the generator polynomial $g(x) = (x+\alpha^0)(x+\alpha^1)...(x+\alpha^{15})$ and the primitive polynomial $p(x) = x^8+x^4+x^3+x^2+1$. Derandomization of the data stream is performed to undo the energy dispersal function inserted at the encoder and is based on the generator $1+x^{14}+x^{15}$.

The QAM receiver is extensively tested and deployed in cable channel environments. Figure 4 illustrates the receiver in 256-QAM mode for a channel corrupted with ISI as well as RFI that is 10dB above the signal power spectral density. The resulting 256-QAM constellation exhibits a slicer SNR of 38dB with zero errors after FEC. Figure 5 illustrates a 1024-QAM constellation with an SNR of 41dB. At a 7Mbaud symbol rate, the throughput using 1024-QAM is 70Mb/s. A representative plot of bit error rate (BER) versus Eb/No for 64-QAM and 256-QAM is illustrated in Figure 6. Implementation loss is measured to be 0.3dB and 1.0dB for 64-QAM and 256-QAM respectively at a BER of 10^{-6}. The receiver IC is packaged in a 100 pin PQFP package, has 650k devices and occupies a die area of 46.9mm². Power dissipation is 1.8W at 5V and 7MBaud operation.

Acknowledgments:

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References:

[1] Bult, K., A. Buchwald, J. Laskowski, "A 170mW 10b 50MSample/s CMOS ADC in 1mm²," ISSCC Digest of Technical Papers, pp. 136-137, Feb., 1997.

[2] Wong, B., H. Samueli, "A 200MHz All-Digital QAM Modulator and Demodulator in 1.2µm CMOS for Digital Radio Applications," IEEE J. Solid-State Circuits, pp.1970-1980, Dec., 1991.

[3] Ramstad, T., "Digital Methods for Conversion Between Arbitrary Sampling Frequencies," IEEE Trans. on Acoustics, Speech, and Signal Processing, vol. ASSP-32, no. 3, pp. 577-591, June, 1984.

[4] Tan, L., H. Samueli, "A 200-MHz Quadrature Digital Synthesizer/Mixer in 0.8µm CMOS," IEEE J. Solid-State Circuits, pp.193-200, Mar., 1995.

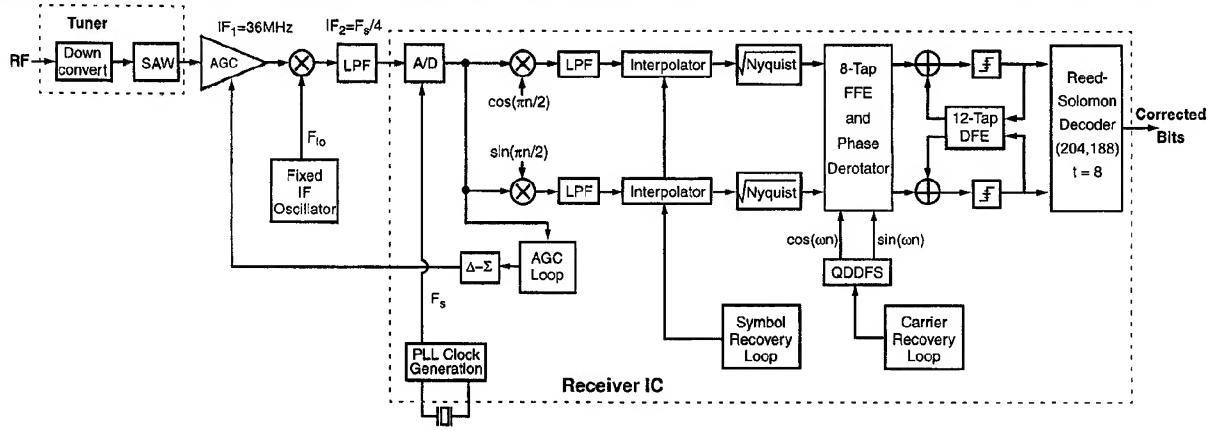

Figure 1: Top level architecture of integrated QAM receiver.

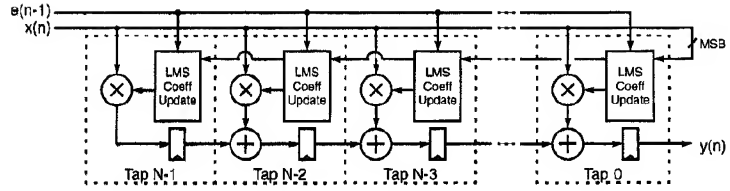

Figure 2: Transpose-form adaptive FIR filter.

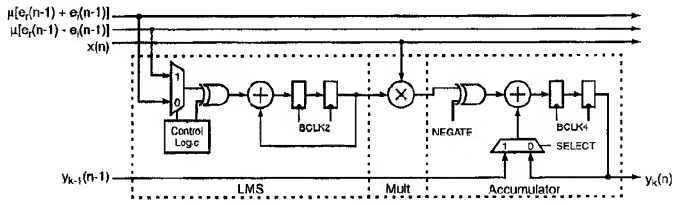

Figure 3: Adaptive tap architecture.

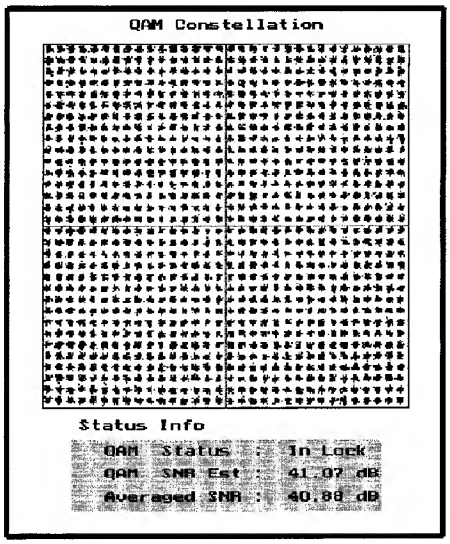

Figure 5: Measured 1024-QAM constellation.

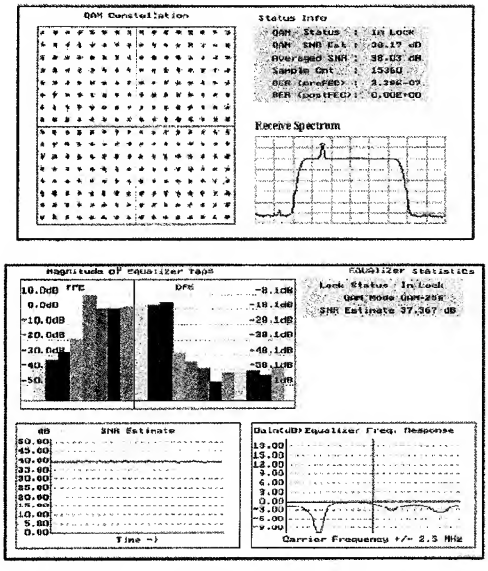

Figure 4: Receiver console: 256-QAM constellation with ISI and RFI.

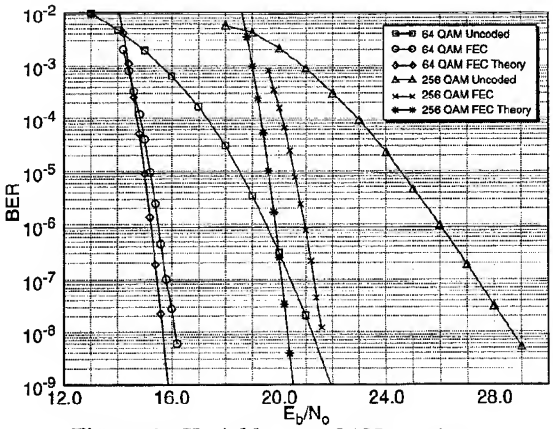

Figure 6: Variable-rate QAM receiver measured coded and uncoded performance.

Figure 7: **See page 438.**

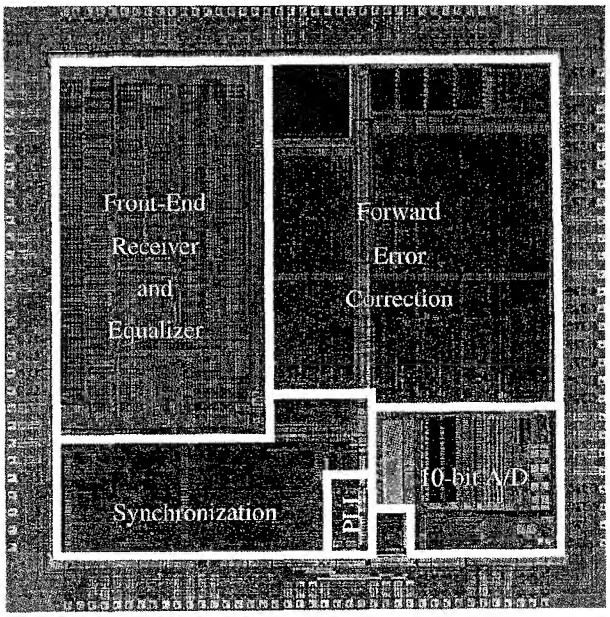

Figure 7: QAM receiver chip micrograph.

FP 13.4: A 3.3V 20-Channel 500Mb/s/ch Optical Receiver with Integrated Optical Detectors

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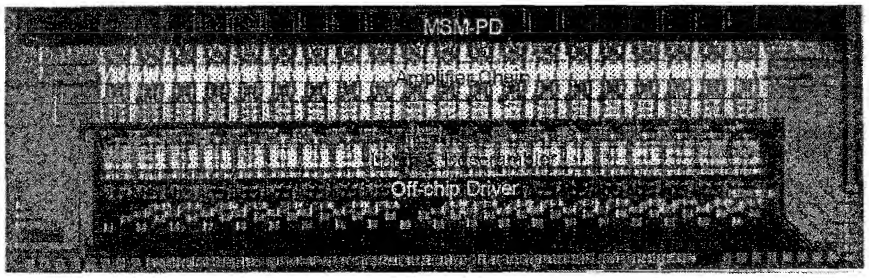

Figure 7: Chip micrograph.